What is Claimed is:

[c1] A semiconductor integrated circuit device comprising:

a die connected to a ground lead and a power lead;

a ground plane connected to the ground lead;

a decoupling capacitor having a first end and a second end, the first end connected to the ground lead and the second end connected to the power lead; and

an encapsulating material for encapsulating the die, the ground plane, and the decoupling capacitor.

[c2] The semiconductor integrated circuit device according to Claim 1, wherein a first plane facing a printed circuit board for mounting electronic parts and a second plane facing opposite to said printed circuit board for mounting electronic parts in said semiconductor integrated circuit device are defined as a bottom surface and a top surface, respectively, and said ground plane extends along said bottom surface.

[c3] The semiconductor integrated circuit device according to Claim 2, wherein said ground plane extends in two dimensions substantially throughout said bottom surface.

[c4] The semiconductor integrated circuit device according to Claim 3, wherein an intra-package wiring substrate comprising wirings for a connecting path between the ground and power leads and bonding pads of the die is disposed between the die and the ground plane, and the decoupling capacitor is connected to the ground plane at one end and the power line of the intra-package wiring substrate at the other end.

[c5] The semiconductor integrated circuit device according to Claim 3, wherein the portion of the encapsulating material for inserting the power lead is connected to a power supply bonding pad of the die through a bonding wire at the die-side end, and the first end of the decoupling capacitor is connected to the ground plane and the second end of the decoupling capacitor is connected to the specified location of said portion for inserting the power lead.

[c6] The semiconductor integrated circuit device according to Claim 5, wherein the specified location of the portion for inserting the power lead to which the decoupling capacitor is connected is the die-side end of the portion for inserting the power lead.

[c7] The semiconductor integrated circuit device according to Claim 5, wherein the ground

plane is connected to the die-side end of the portion for inserting the power lead into the encapsulating material.

[c8] The semiconductor integrated circuit device according to Claim 1, wherein a layer of a material having a lower dielectric constant than the dielectric constant of the encapsulating material is provided between the die and the ground plane.

[c9] The semiconductor integrated circuit device according to Claim 1, further comprising:

a printed circuit board for mounting electronic parts whereon the semiconductor integrated circuit device is mounted; and

an external decoupling capacitor provided on the printed circuit electrically connected in parallel with the decoupling capacitor of the semiconductor integrated circuit device.

[c10] An electronic apparatus or control apparatus comprising a semiconductor integrated circuit device according to Claim 1.

add A2

add B2

ADD C3